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BACKGROUND OF THE INVENTION

Field of the Invention

6 The invention relates generally to the field of integrated
B1 circuit devices and more particularly to the structure of
5 integrated circuit devices.

Background Information

10 The use of metal gate technology is viewed as very
desirable for complementary metal oxide semiconductor (CMOS)
device technology scaling below the sub 0.1 micron regime.
Replacing traditional polysilicon gate electrodes with metal or
metal alloy gate electrodes ^{may reduce} ~~can significantly eliminate~~
undesired voltage drops associated with polysilicon gate
electrodes (e.g., polysilicon depletion effect) and improve
device drive current performance. Metal and metal alloy gate
electrodes ^{may} ~~can~~ also reduce the parasitic resistance of the gate
line and allow longer gate runners in high performance
integrated circuit design for applications such as stacked
gates, wordlines, buffer drivers, etc. ^{B2}

20 Conductive materials have different energies measured
conventionally by their Fermi level. As an example, the Fermi
level of a material determines its work function. The intrinsic
Fermi level of an undoped semiconductor is at the middle of the
bandgap between the conduction and valence band edges. In an N-
type doped silicon, the Fermi level is closer to the conduction

band than to the valence band (e.g., about 4.15 electron-volts). In a P-type doped silicon, the Fermi level is closer to the valence band than the conduction band (e.g., about 5.2 electron-volts).

5 Metals or their compounds have been identified that have work functions similar to the work functions of a conventional P-type doped semiconductor substrate. Other metals or their compounds have been identified that have work functions similar to a conventional N-type doped semiconductor substrate.

10 Examples of metals that have a work function similar to P-type doped semiconductor material, include but are not limited to, nickel (Ni), ruthenium oxide (RuO), molybdenum nitride (MoN),
B and tantalum nitride (Ta_N). Examples of metals that have a work
function to N-type doped semiconductor material, include but are
15 not limited to, ruthenium (Ru), zirconium (Zr), niobium (Nb),
B ~~tantalum (Ta), molybdenum silicide (MoSi), and tantalum silicide~~ ^(Ta) silicide
B ~~(TaSi)~~.

Previous^{ly} proposed metal gate CMOS technology has focused on using one type of metal having a Fermi level located in the
20 middle of the conduction and valence band of the silicon substrate (e.g., work function of about 4.7 electron-volts).
One key drawback of mid-bandgap metals, however, is their
B inability to achieve the small threshold voltage (V_T)^{desirable} necessary
for future CMOS technology scaling, without degrading short
25 channel effects.

A complementary metal gate approach with two work functions, optimized for both NMOS and PMOS devices, respectively, thus far has yet to be integrated into a workable process. The simple method to deposit complementary metals, one after the other, would damage the thin gate dielectric during patterning of at least one of the electrodes making the transistor unusable.

What is needed is the incorporation of complementary metal gate electrode technology ^{in CMOS circuits} ~~into a workable process that is~~ scalable for future CMOS technologies.

SUMMARY OF THE INVENTION

A device is disclosed. The device includes a first transistor having a first metal gate electrode overlying a first gate dielectric on a first area of a semiconductor substrate.

5 The first gate electrode has a work function corresponding to the work function of one of P-type silicon and N-type silicon. The device also includes a second transistor complementary to the first transistor. The second transistor has a second metal gate electrode over a second gate dielectric on a second area of the semiconductor substrate. The second metal gate electrode has a work function corresponding to the work function of the other one of P-type silicon and N-type silicon.

BRIEF DESCRIPTION OF THE DRAWINGS

5 **Figure 1** is a schematic side view illustration of a portion of a semiconductor substrate after the processing step of forming shallow trench isolation structures and well regions in the substrate and a gate dielectric over the surface of a substrate in accordance with a first embodiment of the invention.

10 **Figure 2** shows the semiconductor substrate of **Figure 1** after the further processing step of depositing a metal layer over the gate dielectric in accordance with the first embodiment of the invention.

15 **Figure 3** shows the semiconductor substrate of **Figure 1** after the further processing step of masking a portion of the metal layer over a region of the substrate in accordance with the first embodiment of the invention.

Figure 4 shows the semiconductor substrate of **Figure 1** during the processing step of exposing the unprotected portion of the metal layer to a chemically reactive ambient in accordance with the first embodiment of the invention.

20 **Figure 5** shows the substrate of **Figure 1** after the further processing step of reacting the exposed metal layer with the chemically reactive ambient and removing the masking layer in accordance with the first embodiment of the invention.

Figure 6 shows the substrate of **Figure 1** after the further processing step of patterning complementary gate electrodes in adjacent cell regions in accordance with the first embodiment of the invention.

5 **Figure 7** shows the substrate of **Figure 1** after the further processing step of patterning complementary transistors in adjacent cell regions in accordance with the first embodiment of the invention.

10 **Figure 8** shows a schematic side view illustration of the semiconductor substrate of **Figure 1** after the processing steps of forming cell regions with desired dopants in the substrate and forming a gate dielectric, a first metal layer, and a second layer of metal or other material over the top surface of the substrate in accordance with a second embodiment of the invention.

15 **Figure 9** shows the substrate of **Figure 7** after the further processing step of patterning the second layer over one active region of the first metal layer in accordance with the second embodiment of the invention.

20 **Figure 10** shows the substrate of **Figure 7** after the further processing step of reacting the second layer with the first metal layer in accordance with the second embodiment of the invention.

25 **Figure 11** shows the substrate of **Figure 7** after the processing step of forming complementary transistor devices in

adjacent cell regions in accordance with the second embodiment of the invention.

Figure 12 shows a schematic side view illustration of a semiconductor substrate after the processing steps of forming complementary doped cell regions in the substrate and a gate dielectric material, a first metal layer, and a patterned mask over the substrate and shows the processing step of subjecting the unmasked portion of the metal layer to ion implantation in accordance with a third embodiment of the invention.

Figure 13 shows the substrate of **Figure 12** after the processing step of ion implantation and removal of the mask in accordance with the third embodiment of the invention.

Figure 14 shows the substrate of **Figure 12** after the processing step of patterning complementary transistor devices in adjacent cell regions in accordance with the third embodiment of the invention.

Detailed Description of the Invention

A circuit device employing metal gate electrodes tuned for a work function similar to the desired device type is disclosed. The invention is particularly useful for, but not limited to, the utilization of metal gate electrodes in CMOS technology tuned for optimum NMOS and PMOS device performance. The invention offers a workable process for providing integrated complementary metal gate electrode technology that is scalable for future CMOS technologies.

The invention describes metal gate electrodes or their compounds having Fermi levels close to either N-type or P-type doped silicon. It is to be appreciated that the suitable metal may exist at the desired Fermi level in its natural state or by chemical reaction, alloying, doping, etc. One aspect of the invention described herein is directed at workable methods of modifying metals for optimum NMOS and PMOS device performance.

B **Figures 1-7** illustrate an embodiment of a method of forming ^{PMOS and NMOS devices} ~~a CMOS structure~~ utilizing the complementary gate electrode technology of the invention. **Figure 1** shows semiconductor substrate 100, such as a silicon substrate, or epitaxial layer 100 of a semiconductor substrate having active areas or cell regions defined by shallow trench isolation structures 110 formed in substrate or epitaxial layer 100. In this embodiment, shallow trench isolation structures 110 define active areas or cell regions for individual transistor devices.

Figure 1 also shows the formation of wells 105 and 115 in the individual active area or cell region defined by shallow trench isolation structures 110. For example, P-type well 105 is formed in one region of substrate 100 while N-type well 115 is formed in a second region of substrate 100. P-type well 105 is formed by ^{introducing} ~~diffusing~~ a dopant, such as boron, into the substrate. N-type well 115 is formed by ^{introducing} ~~diffusing~~ a dopant, such as arsenic, phosphorous, or antimony into substrate 100. The practices of forming shallow trench isolation structures 110 and wells 105 and 115 are known in the art and are therefore not presented herein.

Figure 1 still also shows substrate 100 after the further processing step of forming a gate dielectric over the surface of substrate 100. Gate dielectric ~~layer~~ 120 may be grown or deposited. An example of gate dielectric material that is typically grown by thermal techniques over substrate 100 is silicon dioxide (SiO₂). It is to be appreciated that, in addition to SiO₂, other gate dielectrics may be used to further optimize the CMOS transistor devices. For example, gate dielectric materials having a high dielectric constant may be utilized if desirable, for example, to increase the capacitance of the gate.

After gate dielectric ~~layer~~ 120 is formed, Figure 2 shows the substrate of Figure 1 after the further processing step of depositing metal layer 130 over the surface of substrate 100. In this embodiment, metal layer 130 is deposited to ^a~~an~~ thickness [a]

of, for example, 500-2000 Å. In the embodiments that are described herein, the physical properties of at least a portion of metal layer 130 will be modified to adjust the work function for optimum NMOS and PMOS device performance. Thus, metal layer 130 will serve in its present state or in a modified state as a gate electrode. Accordingly, the thickness of metal layer 130 is scalable and should be chosen based primarily on integration issues related to device performance. Further, since in many of the embodiments that are described herein, the physical properties of metal layer 130 will be modified, care should be taken to avoid making metal layer 132 too thick so that, when desired, any modification or transformation of metal layer 130 is complete.

Figure 3 shows the substrate of Figure 1 after the further processing step of patterning ^{mask}masking layer 135 over a portion of metal layer 130. In this embodiment, ^{mask}masking layer 135 is patterned over the active area or cell region represented by P-type well 105. Thus, the portion of metal layer 130 over active area or cell region denoted by N-type well 115 is exposed.

In one embodiment, mask layer 135 is an inactive hard mask material. Mask layer 135 material is inactive inasmuch as it will not participate in a chemical reaction with metal layer 130. Suitable inactive mask materials for ^{mask}masking layer 135 include, but are not limited to, SiO₂ and silicon nitride (Si₃N₄).

B In one embodiment, metal layer 130 is tantalum (Ta). One analysis ~~of the work function~~ of tantalum identifies its Fermi level or work function as between 4.15 and 4.25 electron-volts. Thus, tantalum itself may act as a suitable gate electrode material for an N-type device. Accordingly, in this example, metal layer 130 is protected by ^{mask layer 135} ~~hard mask 135~~ over active areas or cell regions denoted by P-type well 105, ^{e.g.} ~~i.e.~~, active areas or cell regions that may accommodate an N-type device. In this example, ^{mask} ~~masking~~ layer 135 is an inactive hard mask such as SiO₂ or Si₃N₄.

As shown in **Figure 4**, substrate 100 is then exposed to an ambient such as ammonia (NH₃) or nitrogen (N₂). The reactive ambient interacts with the exposed areas of metal layer 130 overlying N-type well 115. In the case of a tantalum metal layer, the interaction and reaction between tantalum and NH₃ or N₂ produces a metal layer of tantalum nitride (TaN) over N-type well region 115. A TaN metal layer has a reported work function of 5.41 electron volts, suitable for use as a P-type gate electrode.

a 20 In another embodiment, ^{mask} ~~masking~~ layer 135 may be made of an active material. In this manner, ^{mask} ~~masking~~ layer 135 may inhibit the reaction by a subsequent processing step (e.g., serve as a mask to a subsequent processing step) while itself reacting with metal layer 130 over the active areas or cell regions denoted by P-type well 105. A suitable active mask includes, but is not limited to, undoped polysilicon. Polysilicon may react with

metal layer 130 to form a silicide. In an example of an active mask of polysilicon, metal layer 130 is, for example, molybdenum (Mo). The exposed area of metal layer 130 is exposed to an NH_3 or N_2 ambient as shown in **Figure 4**. The unprotected molybdenum reacts with the ambient to form molybdenum nitride (MoN) that has a reported ^{Fermi level}~~work function~~ of 5.33 electron-volts (P-type). At the same time, through the addition of heat, such as for example, 850°C , polysilicon, ^{mask}~~masking~~ layer 135 reacts with the molybdenum over active areas or cell regions denoted by P-type well 105 to form molybdenum silicide. Molybdenum silicide has a reported ^{Fermi level}~~work function~~ of 4.25 electron-volts (N-type).

Figure 5 shows substrate 100 after the further processing step of removing inactive mask 135 from the area above metal layer 130 over the active area or cell region denoted by P-type well 105. Alternatively, **Figure 5** shows substrate 100 after the further processing step of reacting the exposed portion of metal layer 130 with reactive ambient 138 and the protected portion of metal layer 130 with active mask 135. Accordingly, in either embodiment, **Figure 5** shows a metal layer overlying substrate 100 having tuned ~~or optimum~~ work functions for the particular electrode device that will be used in the respective active area or cell region. For example, **Figure 5** shows a portion of metal layer 130, such as for example tantalum, overlying the active area or cell region denoted by P-type well 105. Metal layer 130, such as for example tantalum, has a work function corresponding to the work function of an N-type device, identifying the availability of a metal gate electrode with a

tuned work function for an NMOS device in connection with P-type well 105. Conversely, **Figure 5** shows metal layer 132 over an active area or cell region denoted by N-type well 115. Metal layer 132 was formed by the reaction of metal layer 130 with reactive ambient 138 as described above. Metal layer 132 is, for example, tantalum nitride (TaN) having a ^{Fermi level} ~~work function~~ of 5.41 electron-volts. Thus, metal layer 132 is tuned or optimized for a gate electrode of a PMOS device associated with N-type well 115.

Figure 6 shows substrate 100 after the further processing step of patterning the individual metal layers 130 and 132 over their respective device regions. As shown in **Figure 6**, N-type metal layer 130 is formed into metal gate electrode 130 over the region of substrate 100 occupied by P-type well 105. P-type metal layer 132 is patterned into P-type gate electrode 132 over an area of substrate 100 occupied by N-type well 115. Metal layers 130 and 132 are patterned using conventional techniques such as a plasma etchant. In the case of tantalum and TaN, for example, a suitable etchant is a chlorine-based etch chemistry. Patterned in accordance with electrodes 130 and 132 is gate dielectric 120.

Figure 7 shows substrate 100 after the further processing step of forming diffusion or junction regions in substrate 100 in accordance with the characteristics of the desired device. With respect to the N-type device identified by N-type gate electrode 130 overlying ^{P-type well} ~~P-well~~ 105, N-type diffusion or junction

a regions 133 are formed in ^{p-type well} ~~P-well~~ 105 in accordance with conventional techniques. For example, N-type diffusion or junction regions 133 may be formed adjacent gate electrode 130 and self-aligned to gate electrode 130 by implanting a suitable dopant such as, for example, arsenic, phosphorous, or antimony, into ^{type} ~~P-well~~ 105. Similar processing steps may be used to form P-type regions 134, using a dopant, such as, for example, boron. Once diffusion or junctions regions 133 and 134 are formed, gate isolation spacers 152 of a suitable dielectric may be incorporated around gate electrode 130 and gate electrode ~~132~~ to ~~insulate the individual electrodes of the transistor devices.~~

The process described above with respect to **Figures 1-7** illustrates the process of utilizing metal gate electrodes in CMOS technology tuned for ^{improved} ~~optimum~~ NMOS and PMOS performance. To make a CMOS structure, the NMOS and PMOS devices described above are coupled in an appropriate manner. **Figure 7** illustrates the coupling of NMOS device 141 and PMOS device 142 for an inverter.

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Figures 8-11 illustrate a second process of forming complementary gate electrodes for optimum NMOS and PMOS device performance. In this process, as shown in **Figure 8**, semiconductor substrate or epitaxial layer 100 of a substrate has P-type well 105 and N-type well 115 formed in substrate or epitaxial layer 100 defining active area or cell region by shallow trench isolation structures 110. Overlying substrate 100 is gate dielectric 120 as described above and metal layer 130 deposited to a scalable thickness of, for example,

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B approximately 500-2000 Å. In one embodiment, metal layer 130 is chosen to have an appropriate work function for one of an NMOS gate electrode and a PMOS gate electrode (e.g., ^{a Fermi level of} about 4.1 electrons-volts or 5.2 electron-volts, respectively).

B 5 Alternatively, metal layer 130 may ^{employ} ~~require~~ subsequent modification to tune the material to an appropriate work function for an NMOS device. Deposited over metal layer 130 in **Figure 8** is second metal or other material layer 160.

10 **Figure 9** shows the structure after the further processing step of patterning second metal or other material layer 160 over a portion of metal layer 130. In this case, ^{or other material} second metal layer 160 is patterned over the active area or cell region denoted by N-type well 115. Metal layer 130 overlying P-type well 105 is left exposed.

15 Next, the structure is exposed to a heat treatment, such as for example, a high temperature (e.g., 900-1000°C) or laser anneal, to drive the reaction or combination of second metal or other material layer 160 and metal layer 130 to form a metal alloy or other compound. **Figure 10** shows substrate 100 after
20 the further processing step of subjecting metal layer 130 to a heat treatment and forming a metal alloy or other metal compound over N-type well 115. The metal alloy or metal compound 165 is selected to have an appropriate work function for a PMOS device. Examples of suitable metal alloys or metal compounds formed in
25 the manner described include, but are not limited to, [molybdenum silicide]. ^{p-type material, not n-type material}

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Figure 11 shows substrate 100 after the further processing step of patterning metal layers 130 and 165 into metal gate electrodes and forming NMOS transistor device 161 and PMOS transistor device 162 by a process such as described above with reference to Figures 6 and 7. NMOS transistor device 161 includes doped diffusion or junction regions 170 and PMOS transistor device 162 includes doped diffusion or junction regions 175. Finally, as an example, Figure 11 illustrates the coupling of NMOS transistor device 161 and PMOS transistor device 162 for an inverter.

10 In the process described, second metal layer 160 is described as a metal material that interacts or reacts with metal layer 130 and forms an alloy of metal compound with a desired work function. It is to be appreciated that second metal layer 130 could also be polysilicon. In this manner, the reaction between metal layer 130 and polysilicon layer 160 may be a silicide reaction to form a metal silicide having an appropriate work function. It is also to be appreciated that the process may be reversed. In other words, metal layer 130 could be patterned as a polysilicon layer with second metal layer 160 being an appropriate metal to form a metal silicide in accordance with the invention. One approach where the latter process might be preferred is the situation, for example, where only the NMOS transistor devices of the CMOS circuit utilizes metal gate electrode with an optimized work function (i.e., Fermi level of approximately 4.5 electron-volts). Since, in many CMOS circuits, the performance of the NMOS device is more important than the performance of the PMOS device, the process

described herein offers a workable method of ^{improving} ~~optimizing~~ NMOS device performance while leaving PMOS device performance relatively unchanged. Alternatively, two different metals can be deposited and patterned on the polysilicon layer to form two complementary silicides for the NMOS device and the PMOS device, respectively.

Figures 12-14 shows a third process of tuning the metal gate electrode ^{to improve NMOS and PMOS} ~~of a CMOS circuit to optimum~~ device performance by a process generally described as ion mixing. **Figure 12** again shows substrate 100 having P-type well 105 and N-type well 115 formed in substrate 100 or as part of active areas or cell regions defined by shallow trench isolation structures 110. Overlying substrate 100 is gate dielectric ~~layer~~ 120. Overlying gate dielectric 120 is metal layer 130.

Figure 12 shows substrate 100 after the further processing step of adding masking layer 180, such as for example, a hard inactive mask of SiO_2 or Si_3N_4 over that portion of substrate 100 denoted by P-type well 105. In one embodiment, metal layer 130 is chosen, for example, to have a work function corresponding to that of N-type doped silicon ^{a Fermi level of} (i.e., [^]about 4.1 electron-volts). In this manner, metal layer 130 may be patterned over the active area or cell region associated with P-type well 105 to form an NMOS device with a gate electrode tuned for optimum device performance. Alternatively, masking layer 180 may be an active mask, such as for example, a polysilicon, that may react with metal layer 130 in the presence of heat to

form a metal silicide having a work function corresponding to the work function of N-type doped silicon.

5 **Figure 12** shows the further processing step of subjecting the exposed portion of metal layer 130 to an ion implantation 185. The ion implantation step seeks to implant a dosage of ions into the exposed portion of metal layer 130 to modify the work function of metal layer 130. In the embodiment presented, for example, ions are implanted and the implanted metal is annealed (by heat or laser) to modify the work function of metal layer 130 material into a P-type work function metal layer material. **Figure 13** shows substrate 100 after the further processing step of implanting a sufficient dosage of ion to modify the work function of metal layer 130 over active area or cell region denoted by N-type well 115. The modified metal is represented by P-type metal layer 190.

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Figure 14 shows substrate 100 after the further processing step of forming NMOS^{transistor} device 191 and PMOS^{transistor} device 192 utilizing tuned metal gate electrode 130 and 190 over an active area or cell region denoted by P-type well 105 and N-type well 115, respectively. NMOS^{transistor} device 191 includes metal gate electrode 130 having a work function corresponding approximately to the work function of the N-type doped silicon, with N-type doped diffusion or junction region 495. Similarly, PMOS device 192 has metal gate electrode 190 having a work function corresponding approximately to the work function of P-type doped silicon with P-type~~d~~ doped silicon diffusion or junction region

200 formed in substrate. Finally, **Figure 14**, as an example, illustrates the coupling of NMOS transistor device 191 and PMOS transistor device 192 for an inverter.

5 The above discussion presented various ways of turning metal gate electrode for ^{improved} ~~optimum~~ NMOS and PMOS device performance. The invention is particularly useful for, but are not limited to, the utilization of metal gate electrode in CMOS technology. The above discussion assumed that the gate electrode patterning is done after the modification of the metal layer. It is to be appreciated that the same modification of metal material may be accomplished by patterning the gate electrode first and modifying the gate electrode properties afterwards. Whichever sequence is better depends on how the process is integrated into the entire fabrication process.

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20 In the preceding detailed description, the invention is described with reference to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.